outputted based on detected data of the foreign particle defects on the substrate.

15. A semiconductor processing system, comprising:

at least one processing apparatus to process a substrate, the at least one processing apparatus being a component of the semiconductor processing system;

at least one detecting unit which is attached to said at least one processing apparatus and detects foreign particle defects on the substrate; and

a determining unit to determine a foreign particle generating condition from data of the detecting unit.

16. A semiconductor processing system according to claim 15, wherein the foreign particle defects on the substrate are detected by the detecting unit attached to said at least one processing apparatus after transferring the substrate by a transfer unit from said at least one processing apparatus.

17. A semiconductor processing system, comprising:

at least one processing apparatus to process a substrate, the at least one processing apparatus being a component of the semiconductor processing system;

a detecting unit which is attached to said at least one processing apparatus and detects foreign particle defects on

the substrate; and

a foreign particle control system which receives foreign particle data detected by the detecting unit.

18. A semiconductor processing system according to claim 17, wherein the foreign particle defects on the substrate are detected by the detecting unit attached to said at least one processing apparatus after transferring of the substrate by a transfer unit from said at least one processing apparatus.

19. A semiconductor processing system according to claim 17, wherein the foreign particle control system outputs information for control of the foreign particles.

20. A semiconductor processing method comprising the steps of:

detecting foreign particle defects on a substrate during processing of the substrate in a semiconductor fabrication line by a foreign particle detecting unit attached to one processing apparatus of the semiconductor fabrication line; and

determining the foreign particle generation condition of the semiconductor fabrication line.

21. A semiconductor processing method according to claim

20, wherein the semiconductor fabrication line includes a plurality of processing units, each processing unit for performing a single processing of the substrate, the step of detecting being effected by the foreign particle detecting unit attached to the one processing apparatus and after the detection, the substrate is transferred to another processing apparatus which performs a process subsequent to a process of the one processing apparatus.

22. A semiconductor processing method comprising the steps of:

processing a substrate with a first processing apparatus which is a component of a semiconductor fabricating system;

transferring the substrate from the first processing apparatus to a foreign particle detection unit attached to the first processing apparatus;

detecting foreign particle defects on a substrate by the foreign particle detection unit;

transferring the substrate from the foreign particle detection unit to a second processing apparatus which is a component of the semiconductor fabricating system; and

processing the substrate with the second processing apparatus.

23. A semiconductor processing method according to claim

22, wherein the foreign particle defect is detected by detecting a predetermined area of the substrate.

Cont'd A2

24. A semiconductor processing method according to claim 22, wherein the foreign particle defect is detected by a linear image sensor.

25. A semiconductor processing method according to claim 22, wherein the first processing apparatus is an etching apparatus.--

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REMARKS

By the above amendment, in the section "Cross-Reference to Related Applications", the Serial Number of one of the earlier applications for which benefit has been claimed under 35 U.S.C. §120 which is now U.S. Patent No. 5,233,191 has been corrected, while clarifying the relationship of applications. Furthermore, new claims 12-25 have been presented.

Turning to the rejection of claims 1-11 under 35 U.S.C. §103(a) as being unpatentable over Tsuji et al (5,861,952), this rejection is traversed, and reconsideration and withdrawal of the rejection are respectfully requested.

At the outset, applicants note that as listed at page 1 of this application, this application is a continuation application of prior applications, the earliest of the